IFW

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Sumio OGAWA, et al.

Docket No: Q92356

Appln. No.: 10/564,626

Group Art Unit: Not Yet Assigned

Confirmation No.: Not Yet Assigned

Examiner: Not Yet Assigned

Filed: January 13, 2006

For: SEMICONDUCTOR MEMORY DEVICE

SUBMISSION OF INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

For the Examiner's convenience, enclosed herewith is a copy of the English translation of the International Preliminary Report on Patentability (IPRP). It is assumed that copies of the cited references as required by §371(c) will be supplied directly by the International Bureau, but if further copies are needed, the undersigned will undertake to provide them upon request.

Respectfully submitted,

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WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Date: June 21, 2006

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF TRANSMITTAL
OF COPIES OF TRANSLATION
OF THE INTERNATIONAL PRELIMINARY REPORT
ON PATENTABILITY
(CHAPTER I OR CHAPTER II
OF THE PATENT COOPERATION TREATY)
(PCT Rules 44*bis*.3(c) and 72.2)

To:

KUDOH, Minoru
6F, Kadoya Bldg.
24-10, Minamiool 6-chome
Shinagawa-ku, Tokyo 1400013
JAPON

Date of mailing *(day/month/year)* 26 May 2006 (26.05.2006)	
Applicant's or agent's file reference 04PCFP1015	**IMPORTANT NOTIFICATION**
International application No. PCT/JP2004/009959	International filing date *(day/month/year)* 13 July 2004 (13.07.2004)
Applicant ELPIDA MEMORY, INC. et al	

1. **Transmittal of the translation to the applicant.**

☑ The International Bureau transmits herewith a copy of the English translation of the international preliminary report on patentability (Chapter I).

☐ The International Bureau transmits herewith a copy of the English translation of the international preliminary report on patentability (Chapter II).

2. **Transmittal of the copy of the translation to the designated or elected Offices.**

The International Bureau notifies the applicant that copies of that translation have been transmitted to the following designated or elected Offices requiring such translation:

None

The following designated or elected Offices, having waived the requirement for such a transmittal at this time, will receive copies of that translation from the International Bureau only upon their request:

AE, AG, AL, AM, AP, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EA, EC, EE, EG, EP, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OA, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW

3. **Reminder regarding translation into (one of) the official language(s) of the elected Office(s).**

The applicant is reminded that, where a translation of the international application must be furnished to an elected Office, that translation must contain a translation of any annexes to the international preliminary report on patentability (Chapter II).

It is the applicant's responsibility to prepare and furnish such translation directly to each elected Office concerned within the applicable time limit (Rule 74.1). See Volume II of the PCT Applicant's Guide for further details.

The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland	Authorized officer Masashi Honda
Facsimile No.+41 22 740 14 35	Facsimile No.+41 22 338 70 10

Form PCT/IB/338 (January 2004)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY
(Chapter I of the Patent Cooperation Treaty)

(PCT Rule 44*bis*)

Applicant's or agent's file reference 04PCFP1015	**FOR FURTHER ACTION**	See item 4 below
International application No. PCT/JP2004/009959	International filing date *(day/month/year)* 13 July 2004 (13.07.2004)	Priority date *(day/month/year)* 15 July 2003 (15.07.2003)
International Patent Classification (8th edition unless older edition indicated) See relevant information in Form PCT/ISA/237		
Applicant ELPIDA MEMORY, INC.		

1. This international preliminary report on patentability (Chapter I) is issued by the International Bureau on behalf of the International Searching Authority under Rule 44 *bis*.1(a).

2. This REPORT consists of a total of 8 sheets, including this cover sheet.

   In the attached sheets, any reference to the written opinion of the International Searching Authority should be read as a reference to the international preliminary report on patentability (Chapter I) instead.

3. This report contains indications relating to the following items:

☒	Box No. I	Basis of the report
☐	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☒	Box No. VI	Certain documents cited
☐	Box No. VII	Certain defects in the international application
☒	Box No. VIII	Certain observations on the international application

4. The International Bureau will communicate this report to designated Offices in accordance with Rules 44*bis*.3(c) and 93*bis*.1 but not, except where the applicant makes an express request under Article 23(2), before the expiration of 30 months from the priority date (Rule 44*bis* .2).

	Date of issuance of this report 15 May 2006 (15.05.2006)
The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland	Authorized officer Masashi Honda
Facsimile No. +41 22 740 14 35	Telephone No. +41 22 338 70 10

Form PCT/IB/373 (January 2004)

PATENT COOPERATION TREATY

TRANSLATION

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

	Date of mailing *(day/month/year)*
Applicant's or agent's file reference 04PCFP1015	FOR FURTHER ACTION See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/JP2004/009959	13.07.2004	15.07.2003

International Patent Classification (IPC) or both national classification and IPC

Applicant
ELPIDA MEMORY, INC.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☒ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

CORRECTED VERSION

2. FURTHER ACTION

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA/JP	Authorized officer
Facsimile No.	Telephone No.

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/JP2004/009959

Box No. I Basis of this opinion

1. With regard to the language, this opinion has been established on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

☐ This opinion has been established on the basis of a translation from the original language into the following language _____, which is the language of a translation furnished for the purposes of international search (under Rule 12.3 and 23.1(b)).

2. With regard to any nucleotide and/or amino acid sequence disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:

a. type of material

☐ a sequence listing

☐ table(s) related to the sequence listing

b. format of material

☐ in written format

☐ in computer readable form

c. time of filing/furnishing

☐ contained in the international application as filed.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority for the purposes of search.

3. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table(s) relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

4. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No. PCT/JP2004/009959

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-12	YES
	Claims		NO
Inventive step (IS)	Claims	5, 6, 8-10	YES
	Claims	1-4, 7, 11, 12	NO
Industrial applicability (IA)	Claims	1-12	YES
	Claims		NO

2. Citations and explanations:

Document 1: JP 2002-367393 A (Samsung Electronics Co., Ltd.), 20 December 2002, Par. Nos. 0010 to 0037, 0043 to 0060; Figs. 1 to 7 & US 2002/196684 A1 & KR 2002/092520 A

Document 2: JP 2004-039098 A (Kabusbiki Kaisha Runesasu Technology), 05 February 2004, Par. Nos. 0019 to 0066; Figs. 1 to 6 & US 2004/0004866 A1

Claims 1-4

The inventions described in claims 1-4 do not appear to involve an inventive step based on document 1 cited in the ISR.

The "submemory cell array block MCA" and "subredundant memory cell array block RMCA," described in document 1 (Par. No. 0011) correspond to the "memory block" and "redundancy memory block," respectively, described in claim 1.

The structure of "providing one redundant memory cell array block RBLK for all of the memory cell array blocks BLK1 through BLK4," described in document 1 (Fig. 1 and Par. No. 0013) is different from "a plurality of redundancy memory blocks corresponding to each of the plurality of memory blocks," described in claim 1; however, because document 1 states that "the structure may include redundant memory array blocks for each of the memory cell array blocks BLK1 through BLK4" (on Fig. 1 and Par. No. 0013) structuring in the same manner as the "a plurality of redundancy memory blocks corresponding to each of the plurality of memory blocks," stated in claim 1, could be obtained easily by a person skilled in the art.

Document 1 (Fig. 2) describes a structure wherein one or more memory cells (MC1 through MCY) are adjacent to a first subword line (for example, WL11), and describes "substituting a redundant subword line RWL1 for a subword line WL11 wherein a failure has occurred" (in Fig. 2 and Par. No. 0055), so a structure wherein one or more memory cells (MC1 through MCY) are adjacent to and connected to one subword line (for example, WL11) described in Fig. 2 of document 1 corresponds to the structure of "having one or more adjacent memory cell rows or columns be a segment, which is a unit assigned for replacement" in claim 2.

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/JP2004/009959

Box No. VI Certain documents cited

1. Certain published documents (Rule 43*bis*.1 and 70.10)

Application No. Patent No.	Publication date (day/month/year)	Filing date (day/month/year)	Priority date (valid claim) (day/month/year)
JP 2002-194597 [E, Y]	05.02.2004	03.07.2002	

2. Non-written disclosures (Rule 43*bis*.1 and 70.9)

Kind of non-written disclosure	Date of non-written disclosure (day/month/year)	Date of written disclosure referring to non-written disclosure (day/month/year)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/JP2004/009959

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

1. The description of claim 1 of "address bits that are each selected from said plurality of memory blocks and address bits that are each selected from said plurality of redundancy memory blocks are different" is unclear whether the difference is in having different bit lengths of the "address bits" or the positions of the corresponding "address bits."

2. The description of "adjacent to said word line or bit line" in claim 11 is unclear as to what is adjacent to what.

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No. PCT/JP2004/009959

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of: Box V

Document 1 describes that "first decoding signals PRA11, PRA12, PRA12, PRA13, and PRA14 are each mapped selectively to the first decoding signals PX1 - PX4" (in Par. No. 0044) to "substitute to redundant memory cells connected to redundant word lines that have other first decoding signals when, at the time that defective subword lines or defective memory cells that are connected to subword lines cannot be replaced with redundant memory cells that are connected to redundant subword lines that have the same first decoding signals" (in Par. No. 0060).

Here the "redundant memory cell connected to a redundant subword line that has the same first decoding signal" and the "redundant memory cell connected to a redundant subword line that has a different first decoding signal" are each provided with different "subredundant memory cell array blocks RMCA" (in Fig. 2 and Par. Nos. 0057-0059).

Consequently, the structure of "substituting a redundant memory cell that is connected to a redundant subword line that has a different first decoding signal when it is not possible to substitute a redundant memory cell that is connected to a redundant subword line that has the same first decoding signal when substituting a redundant subword line or a redundant memory cell that is connected to a redundant subword line for a defective memory cell that is connected to a subword line or a subword line wherein a defect has occurred" (see Par. No. 0060) corresponds to the structure in claim 2 of "said segment that adjacent that has a defect is replaced for any of the aforementioned mutually-differing plurality of redundancy memory blocks."

Claims 7, 11, and 12

The inventions according to claims 7, 11, and 12 do not appear to involve an inventive step based on document 1 cited in the ISR.

The structure of "each of the memory cell array blocks BLK1 through BLK4 including redundant memory cell array blocks" (in Fig. 1 and Par. No. 0013) and the structure of "replacing subword lines that have defects or defective memory cells connected to these subword lines for redundant memory cells that are connected to the redundant subword lines that have different first decoder signals correspond, respectively, to the structure of "the redundancy memory block is equipped physically for each memory block, and the structure of "said redundancy memory blocks are assigned in common logically to the aforementioned plurality of memory blocks."

Document 1 (Fig. 2) describes a structure wherein the "lower first decoding signals PX3 and PX4" outputted from the "first row decoder" are connected to the "submemory cell array block MCA" and the "redundant memory cell array RMCA," but the structure of an "address bit" and a "decoder" is the same structure as "inputting, into a decode circuit that selects a redundancy memory block, a plurality of least-significant bits of an address that is inputted into the decoder circuit that selects any of the aforementioned plurality of segments" could be achieved easily by a person skilled in the art.

Claims 5, 6, and 8-10

The inventions described in claims 5, 6, and 8-10 appear to involve an inventive step relative to the documents cited in the ISR.

The structure of "said plurality of segments being assigned sequentially and repetitively

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/JP2004/009959

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of: Box V

to said plurality of redundant memory blocks," stated in claims 5 and 6, and the structure of "the first segment and the second segment of said plurality of segments are mutually adjacent and a first redundancy memory block that is assigned to a first segment, and the second redundancy memory block assigned to the second segment are different redundancy memory blocks, as described in claim 8, are not described in document 1, and these structures cannot be conceived of easily even by a person skilled in the art. The inventions described in claims 5, 6, and 8 provide the distinctive effect of making it possible to recover when defective blocks occur in a group in specific blocks, and reducing the number of fuses for the redundancy selecting circuit.

However, in document 2, which was published prior to the application of the present application and published after a previous application that is the foundation for the priority claims of the present application, describes the structure of "recovering from a defect through changing the address assignments when there is a total of two defective memory cells, one each in the right half and the left half of the same row in the memory cell array, where it is suggested that it is possible to substitute the "right half and left half of the same row in the memory cell array" and the "spare cell" in a repeating sequence.

However, in document 2, which was published prior to the application of the present application and published after a previous application that is the foundation for the priority claims of the present application, describes the structure of "recovering from a defect through changing the address assignments when there is a total of two defective memory cells, one each in the right half and the left half of the same row in the memory cell array, where it is suggested that it is possible to substitute the "right half and left half of the same row in the memory cell array" and the "spare cell" in a repeating sequence.